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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,654	09/18/2003	David Jia Chen	ROC920030233US1	8565

23334 7590 02/22/2005

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EXAMINER

NGUYEN, LINH M

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AR

Office Action Summary

Application No.

10/665,654

Applicant(s)

CHEN ET AL.

Examiner

Linh M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a response to the Applicants' amendment filed on 01/03/2005. By virtue of this amendment claims 1-14 are presented in the instant application.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claims 1, 9, 10 and 11, the recitation *““wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active”* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Figure 3 only discloses one type of conductivity and not two different types as recited in the claims.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1, 9 and 10, the recitation “ *wherein a drain of a top transistor in the stack is coupled to a first reference voltage, wherein a source of a bottom transistor in the stack is coupled to a second reference voltage, and wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage*” renders the claim indefinite since it is contradictory with the followed limitations “*wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active*”. The claims contain contradictory limitations because they recite that each delay stage includes the different types of transistors (“first conductivity type” and “second conductivity type”) and yet at the same time they recite the top transistor and the bottom transistor having the same type of conductivity based on the drain and source connectivity of the two.

In order for the delay stages to be able to operate at all and to support the limitations “*wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active*” it is suggested to change the claimed limitations as follows “ *wherein a source of a top transistor in*

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the stack is coupled to a first reference voltage, wherein a source of a bottom transistor in the stack is coupled to a second reference voltage, and wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage”.

Clarification/correction is required.

With respect to claim 2, the following recitation renders the claim indefinite “*each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor; wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a source of the last additional transistor is connected to a drain of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack”*”, as indicated in the above paragraph regarding claims 1, 9 and 10, it is necessary for each delay stage to including both types of transistors, n-channel FET and p-channel FET, in order for the delay stages to be enabled to provide a delayed output. The claimed limitations recite only one type of conductivity, it is suggested that the claim should be corrected as follows “*each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor; wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a **drain** of the last additional transistor is connected to a **source** of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack”*”.

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Clarification/correction is required.

With respect to claims 3-6 and 12-14, the recitation “each transistor is a n-channel FET” or “each transistor is a p-channel FET” render the claims indefinite, as indicated in the above paragraph regarding claims 1, 9 and 10, it is necessary for each delay stage to including both types of transistors, n-channel FET and p-channel FET, in order for the delay stages to be able to operate at all and to support the limitations, in independent claims 1, 9, 10 and 11, “*wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active*”.

With respect to claim 11, the recitation “*a first transistor with a drain electrically coupled to a first reference voltage; a last transistor with a source electrically coupled to a second reference voltage; a totem pole of at least two transistors, the totem pole including: a top transistor with a drain electrically coupled to a source of the transistor;*” renders the claim indefinite since it is contradictory with the followed limitations “*wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active*”. The claims contain contradictory limitations because they recite that each delay stage includes the different types of transistors (“first conductivity type” and “second conductivity type”) and yet at the same time they recite all of the transistors having the same type of conductivity based on their drain and source connectivities.

In order for the delay stages to be able to operate at all and to support the limitations “wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active” it is suggested to change the claimed limitations as follows “a first transistor with a **source** electrically coupled to a first reference voltage; a last transistor with a source electrically coupled to a second reference voltage; a totem pole of at least two transistors, the totem pole including: a top transistor with a **source** electrically coupled to a **drain** of the transistor;”.

Clarification/correction is required.

Claims 7-8 are also rejected under 35 U.S.C. 112, second paragraph because of their dependency on claim 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

5. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798 of record).

With respect to claim 1, 9 and 10, as best understood, Sato et al. discloses, in Fig. 14A, a circuit arrangement comprising a) an input signal [ID1] to be delayed and b) a series of at least two delay stage [60a-60n], wherein each delay stage includes a stack of uniform minimum channel length transistors [P3, N1] selected from one of a first conductivity type [p-channel] and

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a second conductivity type [n-channel], wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage, wherein a source of a top transistor in the stack is coupled to a first reference voltage [V_{cc}], wherein a source of a bottom transistor in the stack is coupled to a second reference voltage [ground], and wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage; wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claim 2, as best understood, Sato et al. discloses, in Fig. 14A, that each stack of transistors includes additional transistors electrically coupled with the top transistor [P3] and the bottom transistor [N1]; wherein a drain of a first additional transistor [P2] is electrically coupled to a source of the top transistor, a **drain** of the last additional transistor [N2] is connected to a **source** of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack, as called for in claim 2;

With respect to claims 3-6, as best understood (see 112 2nd rejection), Song et al. discloses, in Figures 3 and 5 that delay elements comprised both n-channel FET and p-channel FET.

With respect to claims 7 and 8, Song et al. discloses in Figure 3, that the input signal to be delayed is a clock signal.

With respect to claim 11, as best understood, Sato et al. discloses, in Fig. 14A, a delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising a first transistor [P3] with a source electrically coupled to a first reference voltage [Vcc]; a last transistor [N1] with a source electrically coupled to a second reference voltage [Ground]; a totem pole of at least two transistors, the totem pole including: a top transistor [P2] with a source electrically coupled to a drain of the first transistor; a bottom transistor [N2] with a source electrically coupled to a drain of the last transistor and at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a minimum channel length transistor selected from one of a first conductivity type and a second conductivity type; an input electrically coupled to each gate within the totem pole; and an output electrically coupled to connection between one source and one drain of two transistors within the totem pole; wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive: and wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claims 12-14, as best understood (see 112 2nd rejection), Song et al. discloses, in Figures 3 and 5 that delay elements comprised both n-channel FET and p-channel FET.

Remarks and Conclusion

6. Applicant's arguments with respect to claims 1, 3, 4, 9 and 10 filed on 01/03/2005 have been considered but are moot in view of the new ground(s) of rejection due to amendment to the claims.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



LINH MY NGUYEN
PRIMARY EXAMINER